

FORM PTO-1449 <u>INFORMATION DISCLOSURE STATEMENT</u>	ATTY. DOCKET NO. 1875.2790002/RES/GSB	APPLICATION NO. To Be Assigned
	APPLICANT Jan MULDER	
	FILING DATE Herewith (October 21, 2003)	GROUP To Be Assigned

U.S. PATENT DOCUMENTS							
EXAMINER INITIAL		DOCUMENT NUMBER	DATE	NAME	CLASS	SUB-CLASS	FILING DATE
BVO ↓	AA1	6,489,913	12/2002	Hansen et al.	341	156	
	AB1	5,973,632	10/1999	Tai	341	156	
	AC1	6,259,745 B1	07/2001	Chan	375	285	
	AD1	5,191,336	03/1993	Stephenson	341	111	
	AE1						
	AF1						
	AG1						
	AH1						
	AI1						
	AJ1						
	AK1						

FOREIGN PATENT DOCUMENTS							
EXAMINER INITIAL		DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB-CLASS	TRANSLATION
	AL1						Yes No
	AM1						Yes No
	AN1						Yes No
	AO1						Yes No
	AP1						Yes No

OTHER (Including Author, Title, Date, Pertinent Pages, etc.)

BVO	AR	1	Abo, A.M. and Gray, P.R., "A 1.5-V, 10-bit, 14.3-MS/s CMOS Pipeline Analog-to-Digital Converter," <i>IEEE Journal of Solid-State Circuits</i> , IEEE, Vol. 34, No. 5, May 1999, pp. 599-606.				
↓	AS	1	Brandt, B.P. and Lutsky, J., "A 75-mW, 10-b, 20-MSPS CMOS Subranging ADC with 9.5 Effective Bits at Nyquist," <i>IEEE Journal of Solid-State Circuits</i> , IEEE, Vol. 34, No. 12, December 1999, pp. 1788-1795.				
↓	AT	1	Bult, Klaas and Buchwald, Aaron, "An Embedded 240-mW 10-b 50-MS/s CMOS ADC in 1-mm ² ," <i>IEEE Journal of Solid-State Circuits</i> , IEEE, Vol. 32, No. 12, December 1997, pp. 1887-1895.				

EXAMINER <i>B. Mulder</i>	DATE CONSIDERED <i>3/17/04</i>
EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to Applicant.	

FORM PTO-1449 <u>INFORMATION DISCLOSURE STATEMENT</u>	ATTY. DOCKET NO. 1875.2790002/RES/GSB	APPLICATION NO. To Be Assigned
	APPLICANT Jan MULDER	
	FILING DATE Herewith (October 21, 2003)	GROUP To Be Assigned

U.S. PATENT DOCUMENTS							
EXAMINER INITIAL		DOCUMENT NUMBER	DATE	NAME	CLASS	SUB- CLASS	FILING DATE
	AA2						
	AB2						
	AC2						
	AD2						
	AE2						
	AF2						
	AG2						
	AH2						
	AI2						
	AJ2						
	AK2						

FOREIGN PATENT DOCUMENTS							
EXAMINER INITIAL		DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB- CLASS	TRANSLATION
	AL2						Yes No
	AM2						Yes No
	AN2						Yes No
	AO2						Yes No
	AP2						Yes No




OTHER (Including Author, Title, Date, Pertinent Pages, etc.)							
	AR	2	Cho, T.B. and Gray, P.R., "A 10 b, 20 Msample/s, 35 mW Pipeline A/D Converter," <i>IEEE Journal of Solid-State Circuits</i> , IEEE, Vol. 30, No. 3, March 1995, pp. 166-172.				
	AS	2	Choe, M-J. et al., "A 13-b 40-Msamples/s CMOS Pipelined Folding ADC with Background Offset Trimming," <i>IEEE Journal of Solid-State Circuits</i> , IEEE, Vol. 35, No. 12, December 2000, pp. 1781-1790.				
	AT	2	Choi, M. and Abidi, A., "A 6-b 1.3-Gsample/s A/D Converter in 0.35-μm CMOS," <i>IEEE Journal of Solid-State Circuits</i> , IEEE, Vol. 36, No. 12, December 2001, pp. 1847-1858.				

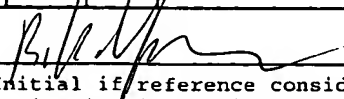
EXAMINER	DATE CONSIDERED 3/17/04
EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to Applicant.	

FORM PTO-1449 <u>INFORMATION DISCLOSURE STATEMENT</u>	ATTY. DOCKET NO. 1875.2790002/RES/GSB	APPLICATION NO. To Be Assigned
	APPLICANT Jan MULDER	
	FILING DATE Herewith (October 21, 2003)	GROUP To Be Assigned

U.S. PATENT DOCUMENTS							
EXAMINER INITIAL		DOCUMENT NUMBER	DATE	NAME	CLASS	SUB- CLASS	FILING DATE
	AA3						
	AB3						
	AC3						
	AD3						
	AE3						
	AF3						
	AG3						
	AH3						
	AI3						
	AJ3						
	AK3						

FOREIGN PATENT DOCUMENTS							
EXAMINER INITIAL		DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB- CLASS	TRANSLATION
	AL3						Yes No
	AM3						Yes No
	AN3						Yes No
	AO3						Yes No
	AP3						Yes No

OTHER (Including Author, Title, Date, Pertinent Pages, etc.)							
	AR	3	Flynn, M. and Sheahan, B., "A 400-Msample/s, 6-b CMOS Folding and Interpolating ADC," <i>IEEE Journal of Solid-State Circuits</i> , IEEE, Vol. 33, No. 12, December 1998, pp. 1932-1938.				
	AS	3	Geelen, G., "A 6b 1.1GSample/s CMOS A/D Converter," <i>IEEE International Solid-State Circuits Conference</i> , IEEE, 2001, pp. 128-129 and 438.				
	AT	3	Hoogzaad, G. and Roovers, R., "A 65-mW, 10-bit, 40-Msample/s BiCMOS Nyquist ADC in 0.8 mm ² ," <i>IEEE Journal of Solid-State Circuits</i> , IEEE, Vol. 34, No. 12, December 1999, pp. 1796-1802.				

EXAMINER 	DATE CONSIDERED 3/17/04
EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to Applicant.	

FORM PTO-1449 <u>INFORMATION DISCLOSURE STATEMENT</u>	ATTY. DOCKET NO. 1875.2790002/RES/GSB	APPLICATION NO. To Be Assigned
	APPLICANT Jan MULDER	
	FILING DATE Herewith (October 21, 2003)	GROUP To Be Assigned

U.S. PATENT DOCUMENTS							
EXAMINER INITIAL		DOCUMENT NUMBER	DATE	NAME	CLASS	SUB-CLASS	FILING DATE
	AA4						
	AB4						
	AC4						
	AD4						
	AE4						
	AF4						
	AG4						
	AH4						
	AI4						
	AJ4						
	AK4						

FOREIGN PATENT DOCUMENTS							
EXAMINER INITIAL		DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB-CLASS	TRANSLATION
	AL4						Yes No
	AM4						Yes No
	AN4						Yes No
	AO4						Yes No
	AP4						Yes No


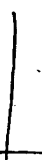

OTHER (Including Author, Title, Date, Pertinent Pages, etc.)			
B/W	AR	4	Hosotani, S. et al., "An 8-bit 20-MS/s CMOS A/D Converter with 50-mW Power Consumption," <i>IEEE Journal of Solid-State Circuits</i> , IEEE, Vol. 25, No. 1, February 1990, pp. 167-172.
I	AS	4	Inginio, J.M. and Wooley, B.A., "A Continuously Calibrated 12-b, 10-MS/s, 3.3-V A/D Converter," <i>IEEE Journal of Solid-State Circuits</i> , IEEE, Vol. 33, No. 12, December 1998, pp. 1920-1931.
↓	AT	4	Ito, M. et al., "A 10 bit 20 MS/s 3 V Supply CMOS A/D Converter," <i>IEEE Journal of Solid-State Circuits</i> , IEEE, Vol. 29, No. 12, December 1994, pp. 1531-1536.

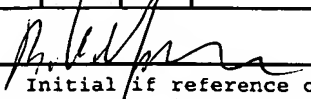
EXAMINER	B. K. [Signature]	DATE CONSIDERED	3/17/04
EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to Applicant.			

FORM PTO-1449 <u>INFORMATION DISCLOSURE STATEMENT</u>	ATTY. DOCKET NO. 1875.2790002/RES/GSB	APPLICATION NO. To Be Assigned
	APPLICANT Jan MULDER	
	FILING DATE Herewith (October 21, 2003)	GROUP To Be Assigned

U.S. PATENT DOCUMENTS							
EXAMINER INITIAL		DOCUMENT NUMBER	DATE	NAME	CLASS	SUB- CLASS	FILING DATE
	AA5						
	AB5						
	AC5						
	AD5						
	AE5						
	AF5						
	AG5						
	AH5						
	AI5						
	AJ5						
	AK5						

FOREIGN PATENT DOCUMENTS							
EXAMINER INITIAL		DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB- CLASS	TRANSLATION
	AL5						Yes No
	AM5						Yes No
	AN5						Yes No
	AO5						Yes No
	AP5						Yes No

OTHER (Including Author, Title, Date, Pertinent Pages, etc.)							
	AR	5	Kattman, K. and Barrow, J., "A Technique for Reducing Differential Non-Linearity Errors in Flash A/D Converters," <i>IEEE International Solid-State Conference</i> , IEEE, 1991, pp. 170-171.				
	AS	5	Kusumoto, K. et al., "A 10-b 20-MHz 30-mW Pipelined Interpolating CMOS ADC," <i>IEEE Journal of Solid-State Circuits</i> , IEEE, Vol. 28, No. 12, December 1993, pp. 1200-1206.				
	AT	5	Lewis, S. et al., "A 10-b 20-Msample/s Analog-to-Digital Converter," <i>IEEE Journal of Solid-State Circuits</i> , IEEE, Vol. 27, No. 3, March 1992, pp. 351-358.				

EXAMINER 	DATE CONSIDERED 3/17/04
EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to Applicant.	

FORM PTO-1449 <u>INFORMATION DISCLOSURE STATEMENT</u>	ATTY. DOCKET NO. 1875.2790002/RES/GSB	APPLICATION NO. To Be Assigned
	APPLICANT Jan MULDER	
	FILING DATE Herewith (October 21, 2003)	GROUP To Be Assigned

U.S. PATENT DOCUMENTS							
EXAMINER INITIAL		DOCUMENT NUMBER	DATE	NAME	CLASS	SUB-CLASS	FILING DATE
	AA6						
	AB6						
	AC6						
	AD6						
	AE6						
	AF6						
	AG6						
	AH6						
	AI6						
	AJ6						
	AK6						

FOREIGN PATENT DOCUMENTS							
EXAMINER INITIAL		DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB-CLASS	TRANSLATION
	AL6						Yes No
	AM6						Yes No
	AN6						Yes No
	AO6						Yes No
	AP6						Yes No




OTHER (Including Author, Title, Date, Pertinent Pages, etc.)			
B/R	AR	6	Mehr, I. and Singer, L., "A 55-mW, 10-bit, 40-Msample/s Nyquist-Rate CMOS ADC," <i>IEEE Journal of Solid-State Circuits</i> , IEEE, Vol. 35, No. 3, March 2000, pp. 318-325.
I	AS	6	Nagaraj, K. et al., "Efficient 6-Bit A/D Converter Using a 1-Bit Folding Front End," <i>IEEE Journal of Solid-State Circuits</i> , IEEE, Vol. 34, No. 8, August 1999, pp. 1056-1062.
✓	AT	6	Nagaraj, K. et al., "A Dual-Mode 700-Msamples/s 6-bit 200-Msamples/s 7-bit A/D Converter in a 0.25-μm Digital CMOS," <i>IEEE Journal of Solid-State Circuits</i> , IEEE, Vol. 35, No. 12, December 2000, pp. 1760-1768.

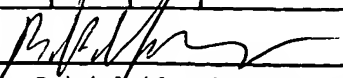
EXAMINER	DATE CONSIDERED 3/17/04
EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to Applicant.	

FORM PTO-1449 <u>INFORMATION DISCLOSURE STATEMENT</u>	ATTY. DOCKET NO. 1875.2790002/RES/GSB	APPLICATION NO. To Be Assigned
	APPLICANT Jan MULDER	
	FILING DATE Herewith (October 21, 2003)	GROUP To Be Assigned

U.S. PATENT DOCUMENTS							
EXAMINER INITIAL		DOCUMENT NUMBER	DATE	NAME	CLASS	SUB-CLASS	FILING DATE
	AA7						
	AB7						
	AC7						
	AD7						
	AE7						
	AF7						
	AG7						
	AH7						
	AI7						
	AJ7						
	AK7						

FOREIGN PATENT DOCUMENTS							
EXAMINER INITIAL		DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB-CLASS	TRANSLATION
	AL7						Yes No
	AM7						Yes No
	AN7						Yes No
	AO7						Yes No
	AP7						Yes No




OTHER (Including Author, Title, Date, Pertinent Pages, etc.)							
	AR	2	Nauta, B. and Venes, A., "A 70-MS/s 110-mW 8-b CMOS Folding and Interpolating A/D Converter," <i>IEEE Journal of Solid-State Circuits</i> , IEEE, Vol. 30, No. 12, December 1995, pp. 1302-1308.				
	AS	2	Pan, H. et al., "A 3.3-V 12-b 50-MS/s A/D Converter in 0.6-μm CMOS with over 80-dB SFDR," <i>IEEE Journal of Solid-State Circuits</i> , IEEE, Vol. 35, No. 12, December 2000, pp. 1769-1780.				
	AT	2	Song, W-C. et al., "A 10-b 20-Msample/s Low-Power CMOS ADC," <i>IEEE Journal of Solid-State Circuits</i> , IEEE, Vol. 30, No. 5, May 1995, pp. 514-521.				

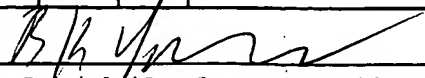
EXAMINER 	DATE CONSIDERED 3/17/04
EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP §09. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to Applicant.	

FORM PTO-1449 <u>INFORMATION DISCLOSURE STATEMENT</u>	ATTY. DOCKET NO. 1875.2790002/RES/GSB	APPLICATION NO. To Be Assigned
	APPLICANT Jan MULDER	
	FILING DATE Herewith (October 21, 2003)	GROUP To Be Assigned

U.S. PATENT DOCUMENTS							
EXAMINER INITIAL		DOCUMENT NUMBER	DATE	NAME	CLASS	SUB- CLASS	FILING DATE
	AA8						
	AB8						
	AC8						
	AD8						
	AE8						
	AF8						
	AG8						
	AH8						
	AI8						
	AJ8						
	AK8						

FOREIGN PATENT DOCUMENTS							
EXAMINER INITIAL		DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB- CLASS	TRANSLATION
	AL8						Yes No
	AM8						Yes No
	AN8						Yes No
	AO8						Yes No
	AP8						Yes No

OTHER (Including Author, Title, Date, Pertinent Pages, etc.)			
	AR	8	Sumanen, L. et al., "A 10-bit 200-MS/s CMOS Parallel Pipeline A/D Converter," <i>IEEE Journal of Solid-State Circuits</i> , IEEE, Vol. 36, No. 7, July 2001, pp. 1048-1055.
	AS	8	Taft, R.C. and Tursi, M.R., "A 100-MS/s 8-b CMOS Subranging ADC with Sustained Parametric Performance from 3.8 V Down to 2.2 V," <i>IEEE Journal of Solid-State Circuits</i> , IEEE, Vol. 36, No. 3, March 2001, pp. 331-338.
	AT	8	van der Ploeg, H. and Remmers, R., "A 3.3-V, 10-b 25-Msample/s Two-Step ADC in 0.35-μm CMOS," <i>IEEE Journal of Solid-State Circuits</i> , IEEE, Vol. 34, No. 12, December 1999, pp. 1803-1811.

EXAMINER 	DATE CONSIDERED 3/17/04
EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to Applicant.	

FORM PTO-1449 <u>INFORMATION DISCLOSURE STATEMENT</u>	ATTY. DOCKET NO. 1875.2790002/RES/GSB	APPLICATION NO. To Be Assigned
	APPLICANT Jan MULDER	
	FILING DATE Herewith (October 21, 2003)	GROUP To Be Assigned

U.S. PATENT DOCUMENTS							
EXAMINER INITIAL		DOCUMENT NUMBER	DATE	NAME	CLASS	SUB-CLASS	FILING DATE
	AA9						
	AB9						
	AC9						
	AD9						
	AE9						
	AF9						
	AG9						
	AH9						
	AI9						
	AJ9						
	AK9						

FOREIGN PATENT DOCUMENTS							
EXAMINER INITIAL		DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB-CLASS	TRANSLATION
	AL9						Yes No
	AM9						Yes No
	AN9						Yes No
	AO9						Yes No
	AP9						Yes No




OTHER (Including Author, Title, Date, Pertinent Pages, etc.)			
BW	AR	2	van der Ploeg, H. et al., "A 2.5-V 12-b 54-Msample/s 0.25- μ m CMOS ADC in 1-mm ² With Mixed-Signal Chopping and Calibration," <i>IEEE Journal of Solid-State Circuits</i> , IEEE, Vol. 36, No. 12, December 2001, pp. 1859-1867.
I	AS	2	Vorenkamp, P. and Roovers, R., "A 12-b, 60-Msample/s Cascaded Folding and Interpolating ADC," <i>IEEE Journal of Solid-State Circuits</i> , IEEE, Vol. 32, No. 12, December 1997, pp. 1876-1886.
V	AT	2	Wang, Y-T. and Razavi, B., "An 8-bit 150-MHz CMOS A/D Converter," <i>IEEE Journal of Solid-State Circuits</i> , IEEE, Vol. 35, No. 3, March 2000, pp. 308-317.

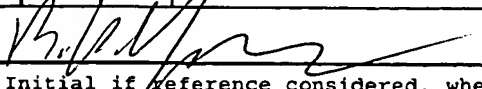
EXAMINER		DATE CONSIDERED	3/17/04
EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to Applicant.			

FORM PTO-1449 <u>INFORMATION DISCLOSURE STATEMENT</u>	ATTY. DOCKET NO. 1875.2790002/RES/GSB	APPLICATION NO. To Be Assigned
	APPLICANT Jan MULDER	
	FILING DATE Herewith (October 21, 2003)	GROUP To Be Assigned

U.S. PATENT DOCUMENTS							
EXAMINER INITIAL		DOCUMENT NUMBER	DATE	NAME	CLASS	SUB- CLASS	FILING DATE
	AA10						
	AB10						
	AC10						
	AD10						
	AE10						
	AF10						
	AG10						
	AH10						
	AI10						
	AJ10						
	AK10						

FOREIGN PATENT DOCUMENTS							
EXAMINER INITIAL		DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB- CLASS	TRANSLATION
	AL10						Yes No
	AM10						Yes No
	AN10						Yes No
	AO10						Yes No
	AP10						Yes No



OTHER (Including Author, Title, Date, Pertinent Pages, etc.)							
	AR	<u>10</u>	Yotsuyanagi, M. et al., "A 2 V, 10 b, 20 Msample/s, Mixed-Mode Subranging CMOS A/D Converter," <i>IEEE Journal of Solid-State Circuits</i> , IEEE, Vol. 30, No. 12, December 1995, pp. 1533-1537.				
	AS	<u>10</u>	Yu, P.C. and Lee, H-S., "A 2.5-V, 12-b, 5-Msample/s Pipelined CMOS ADC," <i>IEEE Journal of Solid-State Circuits</i> , IEEE, Vol. 31, No. 12, December 1996, pp. 1854-1861.				
	AT	<u>10</u>	Miyazaki et al., ISSCC 2002/Session 10/High-Speed ADCs/10.5, "A 16mW 30 MSample/s 10b Pipelined A/D Converter using a Pseudo-Differential Architecture", February 5, 2002, 3 pgs.				

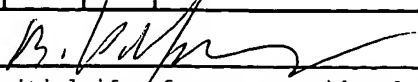
EXAMINER 	DATE CONSIDERED <u>3/17/04</u>
EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to Applicant.	

FORM PTO-1449 <u>INFORMATION DISCLOSURE STATEMENT</u>	ATTY. DOCKET NO. 1875.2790002/RES/GSB	APPLICATION NO. To Be Assigned
	APPLICANT Jan MULDER	
	FILING DATE Herewith (October 21, 2003)	GROUP To Be Assigned

U.S. PATENT DOCUMENTS							
EXAMINER INITIAL		DOCUMENT NUMBER	DATE	NAME	CLASS	SUB- CLASS	FILING DATE
	AA11						
	AB11						
	AC11						
	AD11						
	AE11						
	AF11						
	AG11						
	AH11						
	AI11						
	AJ11						
	AK11						

FOREIGN PATENT DOCUMENTS							
EXAMINER INITIAL		DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB- CLASS	TRANSLATION
	AL11						Yes No
	AM11						Yes No
	AN11						Yes No
	AO11						Yes No
	AP11						Yes No

OTHER (Including Author, Title, Date, Pertinent Pages, etc.)							
	AR	<u>11</u>	Sushihara et al., ISSCC 2002/Session 10/High-Speed ADCs/10.3, "A 7b 450 MSample/s 50mW CMOS ADC in 0.3 mm ² ", February 5, 2002, 3 pgs.				
	AS	<u>11</u>	Dingwall et al., IEEE Journal of Solid-State Circuits, Vol. SC-20, No. 6, "An 8-MHz CMOS Subranging 8-Bit A/D Converter", December 1985, pgs. 1138-1143.				
	AT	<u>11</u>					

EXAMINER 	DATE CONSIDERED <u>3/17/04</u>
EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP §09. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to Applicant.	